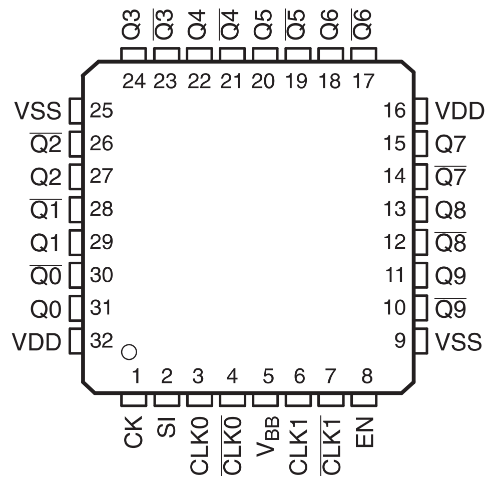
# *Not Recommended for New Designs*
# PROGRAMMABLE LOW-VOLTAGE 1:10 LVDS CLOCK DRIVER

## FEATURES

- **Low-Output Skew <30 ps (Typical) for Clock-Distribution Applications**
- **Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs**
- **$V_{CC}$ range 2.5 V ±5%**
- **Typical Signaling Rate Capability of Up to 1.1 GHz**
- **Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, $\overline{CLK0}$ or CLK1, $\overline{CLK1}$ Inputs**
- **Full Rail-to-Rail Common-Mode Input Range**
- **Receiver Input Threshold ±100 mV**
- **Available in 32-Pin LQFP Package**
- **Fail-Safe I/O-Pins for $V_{DD}$ = 0 V (Power Down)**

**LQFP PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The CDCLVD110 clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0, Q9) with minimum skew for clock distribution. The CDCLVD110 is specifically designed for driving 50-Ω transmission lines.

When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled/disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when EN = 0, the outputs are not programmable and all outputs are enabled.

The CDCLVD110 is characterized for operation from –40°C to 85°C.

***Not Recommended for New Designs. Use CDCLVD110A as a Replacement.***

TEXAS INSTRUMENTS
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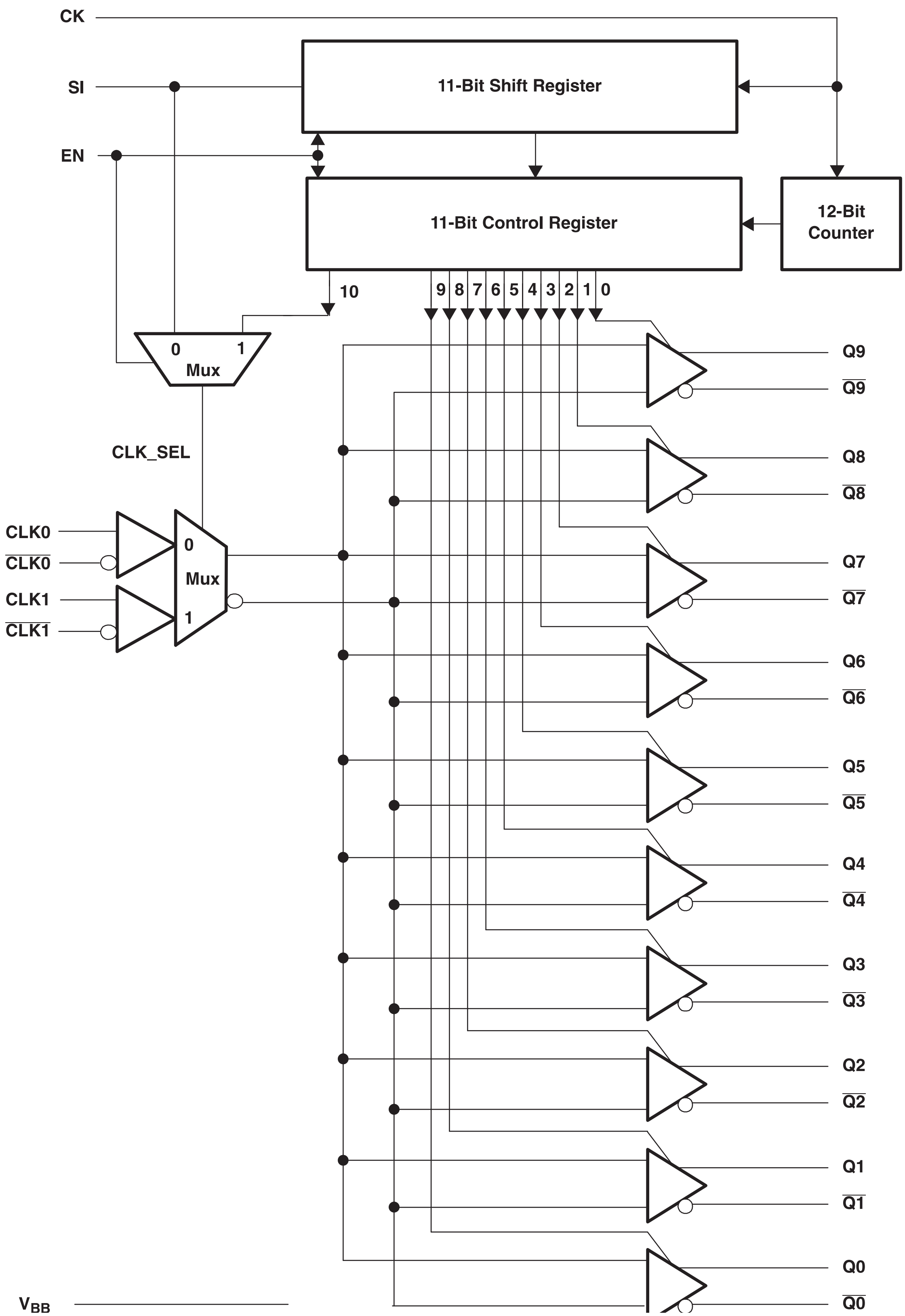
## FUNCTIONAL BLOCK DIAGRAM



## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CK | 1 | I | Control register input clock, features a 120-kΩ pullup resistor |
| SI | 2 | I | Control register serial input/CLK Select, features a 120-kΩ pulldown resistor |
| CLK0 | 3 | I | True differential input, LVDS |
| $\overline{CLK0}$ | 4 | I | Complementary differential input, LVDS |
| $V_{BB}$ | 5 | O | Reference voltage output |
| CLK1 | 6 | I | True differential input, LVDS |
| $\overline{CLK1}$ | 7 | I | Complementary differential input, LVDS |
| EN | 8 | I | Control enable (for programmability), features a 120-kΩ pulldown resistor, input |
| $V_{SS}$ | 9, 25 | | Device ground |
| $V_{DD}$ | 16, 32 | | Supply voltage |
| Q [9:0] | 11, 13, 15, 18, 20, 22, 24, 27, 29, 31 | O | Clock outputs, these outputs provide low-skew copies of CLKIN |
| $\overline{Q[9:0]}$ | 10, 12, 14, 17, 19, 21,23, 26, 28, 30 | O | Complementary clock outputs, these outputs provide low-skew copies of CLKIN |

## ABSOLUTE MAXIMUM RATINGS(1)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.3 to 2.8 | V |
| $V_I$ | Input voltage | –0.2 to ($V_{DD}$ + 0.2) | V |
| $V_O$ | VI Output voltage | –0.2 to ($V_{DD}$ + 0.2) | V |
| Qn, $\overline{Qn}$, $I_{OSD}$ | Driver short circuit current | Continuous | |
| | Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD | >2000 | V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.375 | 2.5 | 2.625 | V |
| $V_{IC}$ | Receiver common-mode input voltage | $0.5\lvert V_{ID}\rvert$ | | $V_{DD} - 0.5\lvert V_{ID}\rvert$ | V |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | |
| $\lvert V_{OD}\rvert$ | Differential output voltage | $R_L$ = 100Ω | 250 | 450 | 600 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ magnitude change | | | | 50 | mV |
| $V_{OS}$ | Offset voltage | –40°C to 85°C | 0.95 | 1.2 | 1.45 | V |
| $\Delta V_{OS}$ | $V_{OS}$ magnitude change | | | | 350 | mV |
| $I_{OS}$ | Output short circuit current | $V_O$ = 0 V | | | –20 | mA |
| | | $\lvert V_{OD}\rvert$ = 0 V | | | 20 | |
| $V_{BB}$ | Reference output voltage | $V_{DD}$ = 2.5 V, $I_{BB}$ = –100 µA | 1.15 | 1.25 | 1.35 | V |
| $C_O$ | Output capacitance | $V_O$ = $V_{DD}$ or GND | | 3 | | pF |

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **RECEIVER** | | | | | | | |
| $V_{IDH}$ | Input threshold high | | | | | 100 | mV |
| $V_{IDL}$ | Input threshold low | | | –100 | | | mV |
| $\|V_{ID}\|$ | Input differential voltage | | | 200 | | | mV |
| $I_{IH}$ | Input current, CLK0/$\overline{CLK0}$, CLK1/$\overline{CLK1}$ | | $V_I = V_{DD}$ | –5 | | 5 | µA |
| $I_{IL}$ | | | $V_I = 0$ V | | | | |
| $C_I$ | Input capacitance | | $V_I = V_{DD}$ or GND | | 3 | | pF |
| **SUPPLY CURRENT** | | | | | | | |
| $I_{DD}$ | Supply current | Full loaded | All outputs enabled and loaded, $R_L = 100\ \Omega$, f = 0 Hz | | | 130 | mA |
| | | No load | Outputs enabled, no output load, f = 0 Hz | | | 35 | |
| $I_{DDZ}$ | | 3-State | All outputs 3-state by control logic, f = 0 Hz | | | 35 | |

## JITTER CHARACTERISTICS

characterized with CDCLVD110 performance EVM, $V_{DD}$ = 3.3 V, OUTPUTS NOT UNDER TEST are terminated to 50Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{jitterLVDS}$ | Additive phase jitter from input to LVDS output Q3 and $\overline{Q3}$ | 12 kHz to 5 MHz, $f_{out}$ = 30.72 MHz | | 650 | | fs rms |
| | | 12 kHz to 20 MHz, $f_{out}$ = 125 MHz | | 299 | | |

## LVDS — SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{DD}$ = 2.5 V ±5%

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay low-to-high | CLK0, $\overline{CLK0}$<br>CLK1, $\overline{CLK1}$ | Qn, $\overline{Qn}$ | | 2 | 3 | ns |
| $t_{PHL}$ | Propagation delay high-to-low | CLK0, $\overline{CLK0}$<br>CLK1, $\overline{CLK1}$ | Qn, $\overline{Qn}$ | | 2 | 3 | ns |
| $t_{duty}$ | Duty cycle | CLK0, $\overline{CLK0}$<br>CLK1, $\overline{CLK1}$ | Qn, $\overline{Qn}$ | 45% | | 55% | |
| $t_{sk(o)}$ | Output skew | | Any Qn, $\overline{Qn}$ | | 30 | | ps |
| $t_{sk(p)}$ | Pulse skew | | Any Qn, $\overline{Qn}$ | | | 50 | ps |
| $t_{sk(pp)}$ | Part-to-part skew | | Any Qn, $\overline{Qn}$ | | | 600 | ps |
| $t_r$ | Output rise time, 20% to 80%, $R_L = 100\ \Omega$, $C_L = 5$ pF | | Any Qn, $\overline{Qn}$ | | | 350 | ps |
| $t_f$ | Output fall time, 20% to 80%, $R_L = 100\ \Omega$, $C_L = 5$ pF | | Any Qn, $\overline{Qn}$ | | | 350 | ps |
| $f_{clk}$ | Max input frequency | CLK0, $\overline{CLK0}$<br>CLK1, $\overline{CLK1}$ | Any Qn, $\overline{Qn}$ | 900 | 1100 | | MHz |

## CONTROL REGISTER CHARACTERISTICS

over recommended operating free-air temperature range, $V_{DD}$ = 2.5 V ±5% (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum frequency of shift register | | 100 | 150 | | MHz |
| $t_{su}$ | Setup time, clock to SI | | | | 2 | ns |
| $t_h$ | Hold time, clock to SI | | | | 1.5 | ns |
| $t_{removal}$ | Removal time, enable to clock | | | | 1.5 | ns |
| $t_w$ | Clock pulse width, minimum | | 3 | | | ns |
| $V_{IH}$ | Logic input high | $V_{DD}$ = 2.5 V | 2 | | | V |
| $V_{IL}$ | Logic input low | $V_{DD}$ = 2.5 V | | | 0.8 | V |

## CONTROL REGISTER CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $V_{DD}$ = 2.5 V ±5% (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input current, CK pin | $V_I = V_{DD}$ | –5 | | 5 | μA |
| | Input current, SI and EN pins | | 10 | | –30 | |
| $I_{IL}$ | Input current, CK pin | $V_I$ = GND | –10 | | 30 | μA |
| | Input current, SI and EN pins | | –5 | | 5 | |

## SPECIFICATION OF CONTROL REGISTER

The CDCLVD110 is provided with an 11-bit, serial-in shift register and an 11-bit control register. The control Register enables/disables each output clock and selects either CLK0 or CLK1 as the input clock. The CDCLVD110 has two modes of operation:

**Programmable Mode (EN=1)**

The shift register utilizes a serial input (SI) and a clock input (CK). Once the shift register is loaded with 11 clock pulses, the twelfth clock pulse loads the control register. The first bit (bit 0) on SI enables the Q9, $\overline{Q9}$ output pair, and the tenth bit (bit 9) enables the Q0, $\overline{Q0}$ pair. The eleventh bit (bit 10) on SI selects either CLK0 or CLK1 as the input clock; a bit value of 0 selects CLK0, whereas a bit value of 1 selects CLK1. To restart the control register configuration, a reset of the state machine must be done with a clock pulse on CK (shift register clock input) and EN set to low. The control register can be configured only once after each reset.

**Standard Mode (EN=0)**

In this mode, the CDCLVD110 is not programmable and all the clock outputs are enabled. The clock input (CLK0 or CLK1) is selected with the SI pin, as is shown in the table entitled control register.

| STATE-MACHINE INPUTS | | | |
|---|---|---|---|
| **EN** | **SI** | **CK** | **OUTPUT** |
| L | L | X | All outputs enabled, CLK0 selected, control register disabled, default state |
| L | H | X | All outputs enabled, CLK1 selected, control register disabled |
| H | L | ↑ | First stage stores L, other stage stores data of previous stage |
| H | H | | First stage stores H, other stage stores data of previous stage |
| L | X | | Reset of state machine, shift and control registers |

| CONTROL REGISTER | | |
|---|---|---|
| **BIT 10** | **BITS [0-9]** | **$Q_N$[0-9]** |
| L | H | CLK0 |
| H | H | CLK1 |
| X | L | Outputs disabled |

| SERIAL INPUT (SI) SEQUENCE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **BIT 10** | **BIT 9** | **BIT 8** | **BIT 7** | **BIT 6** | **BIT 5** | **BIT 4** | **BIT 3** | **BIT 2** | **BIT 1** | **BIT 0** |
| CLK_SEL | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 | Q9 |

| TRUTH TABLE FOR CONTROL LOGIC | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CK** | **EN** | **SI** | **CLK0** | **$\overline{CLK0}$** | **CLK1** | **$\overline{CLK1}$** | **Q(0-9)** | **$\overline{Q(0-9)}$** |
| L | L | L | L | H | X | X | L | H |
| L | L | L | H | L | X | X | H | L |
| L | L | L | Open | Open | X | X | L | H |
| L | L | H | X | X | L | H | L | H |
| L | L | H | X | X | H | L | H | L |
| L | L | H | X | X | Open | Open | L | H |
| All outputs enabled | | X = Don't care | | | | | | |

## APPLICATION INFORMATION

### Fall-Safe Information

For $V_{DD}$ = 0 V (power-down mode) the CDCLVD110 has fail-safe input and output pins. In power-on mode, fail-safe biasing at input pins can be accomplished with a 10-kΩ pullup resistor from CLK0/CLK1 to VDD and a 10-kΩ pulldown resistor from $\overline{\text{CLK0}}$/$\overline{\text{CLK1}}$ to GND.

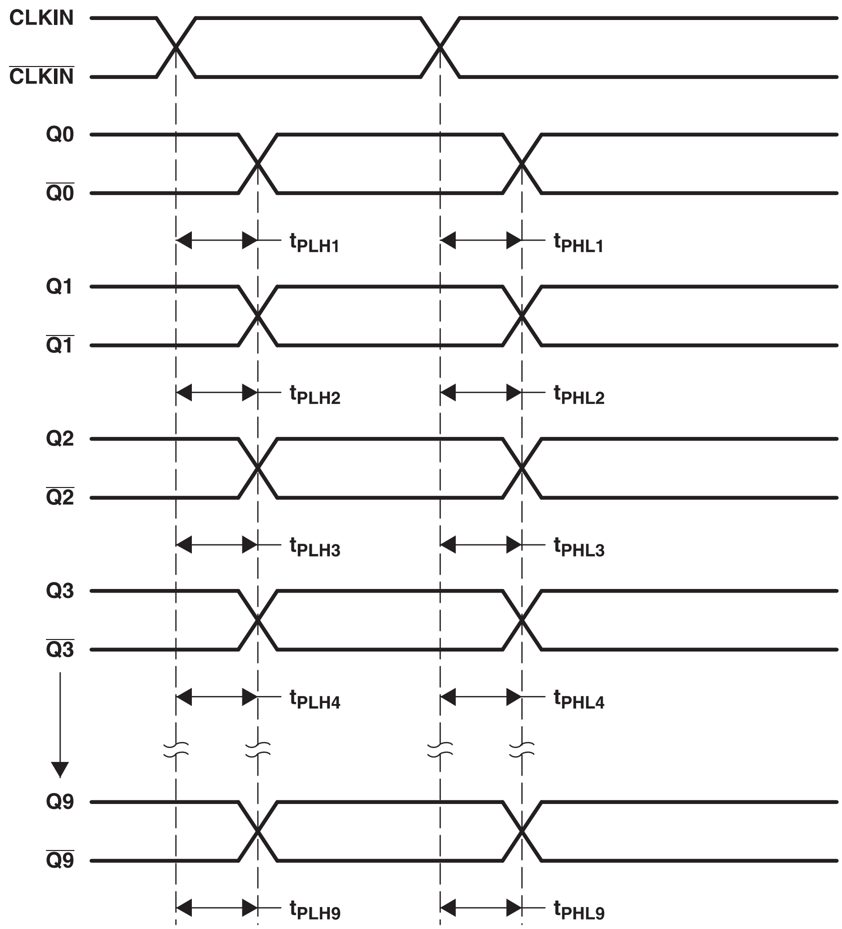
### LVDS Receiver Input Termination

The LVDS receiver inputs need to have 100-Ω termination resistors placed as close as possible across the input pins.

### Control Inputs Termination

No external termination is required. The CK control input has an internal 120-k. pullup resistor while SI- and EN-control inputs each have an internal 120-kΩ pulldown resistor. If the control pins are left open per the default, all outputs are enabled, CLK0, $\overline{\text{CLK0}}$ is selected, and the control register is disabled.

## PARAMETER MEASUREMENT INFORMATION




A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and the slowest $t_{PLHn}$ (n = 1, 2,...10)
– The difference between the fastest and the slowest $t_{PHLn}$ (n = 1, 2,...10)

B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
– The difference between the fastest and the slowest $t_{PLHn}$ (n = 1, 2,...10) across multiple devices
– The difference between the fastest and the slowest $t_{PHLn}$ (n = 1, 2,...10) across multiple devices

C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{PHL}$) and the low-to-high ($t_{PLH}$) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = | t_{PHL} - t_{PLH} |$. Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

**Figure 1. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$**

## PARAMETER MEASUREMENT INFORMATION (continued)

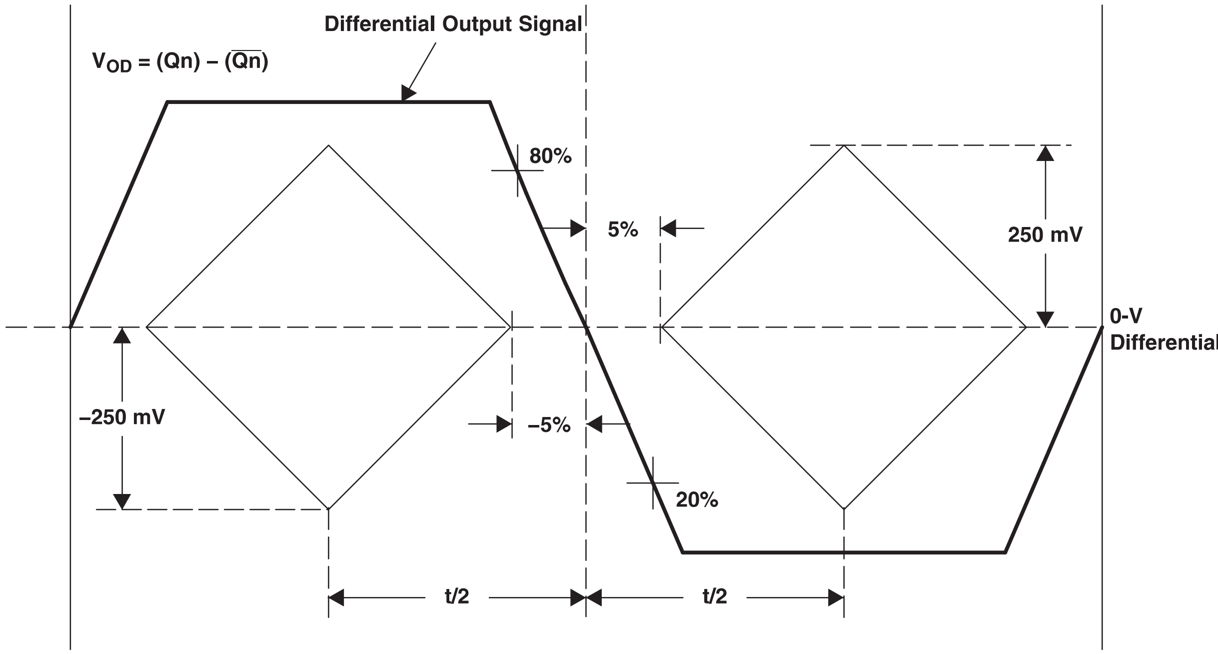



Figure 2. Test Criteria for $f_{clk}$, Duty Cycle, $t_r$, $t_f$, $V_{OD}$

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| CDCLVD110VF | ACTIVE | LQFP | VF | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCLVD110VFG4 | ACTIVE | LQFP | VF | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCLVD110VFR | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCLVD110VFRG4 | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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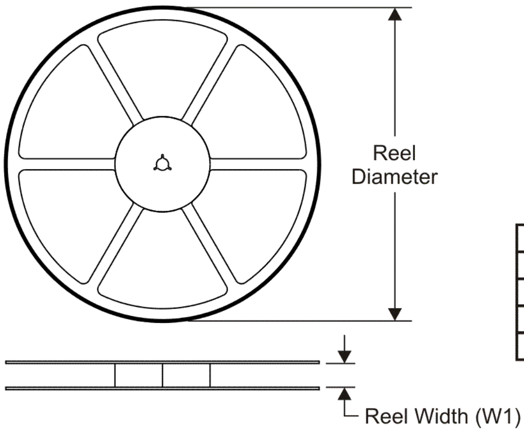
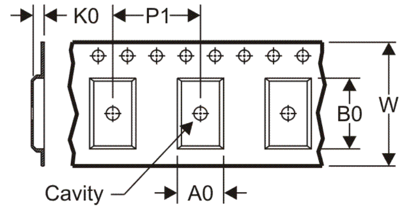
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

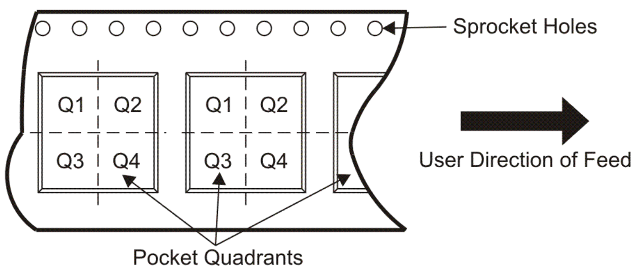



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

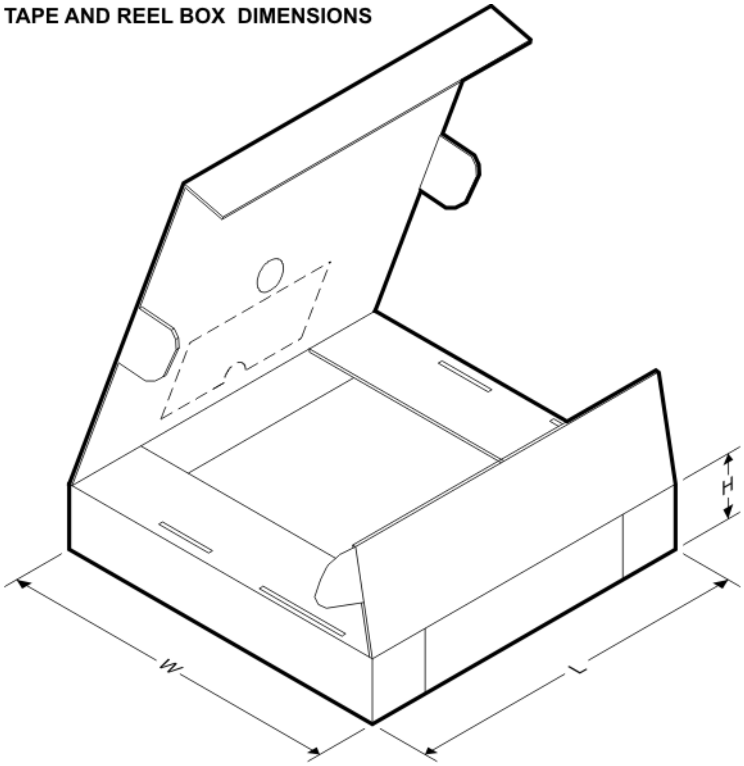
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCLVD110VFR | LQFP | VF | 32 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |

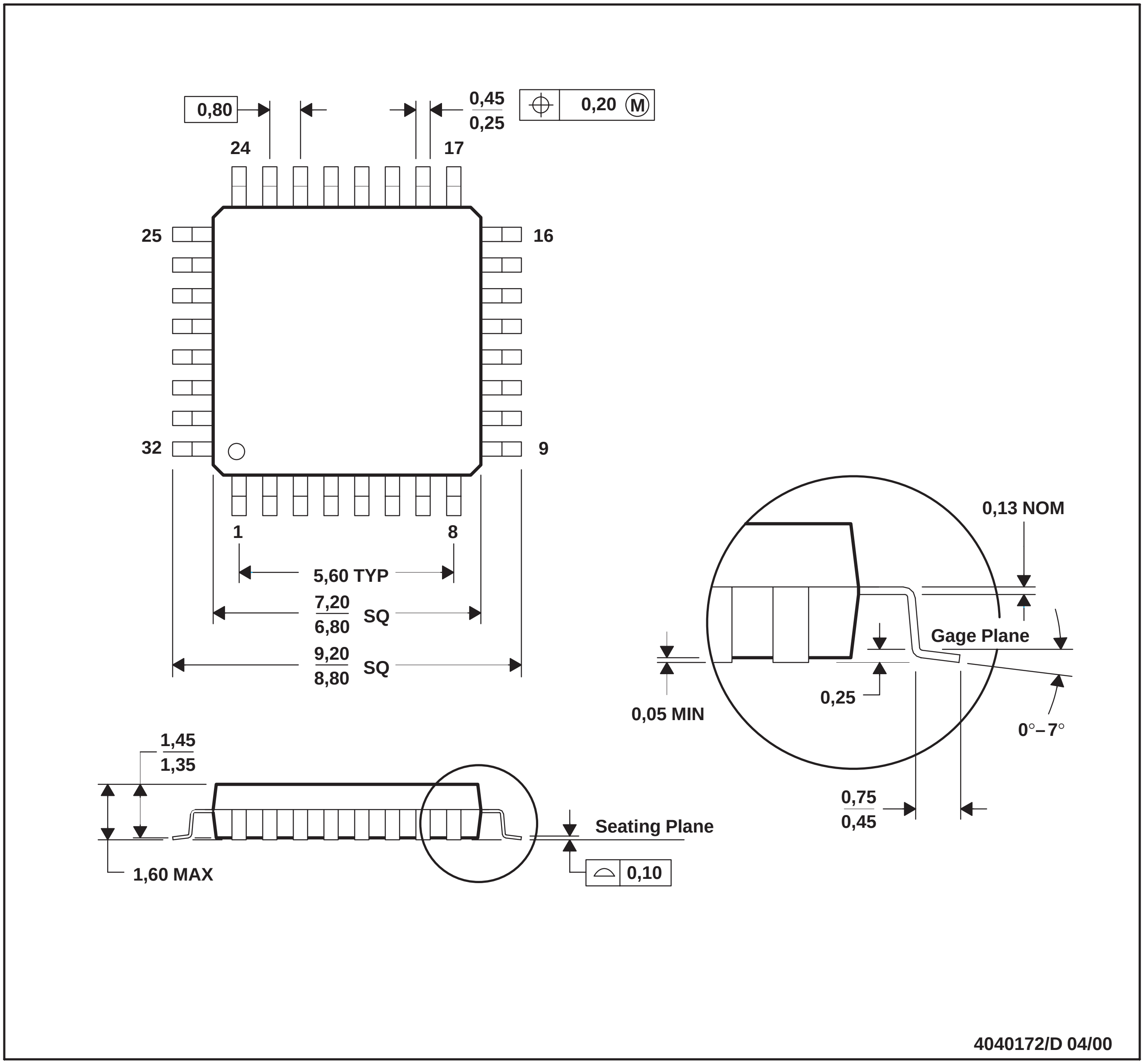
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCLVD110VFR | LQFP | VF | 32 | 1000 | 333.2 | 345.9 | 28.6 |

**VF (S-PQFP-G32)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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